Patent Number : 61007 (R.O.C)
Patent Pending : 83216083 (R.O.C)

GENERAL DESCRIPTION

The EM78248/448 is an 8-bit microprocessor with low-power, high speed CMOS technology. Integrated onto a single chip are on-chip watchdog timer (WDT), RAM, ROM, real time clock/counter, power down mode and bidirectional tri-state I/O ports. It can be developed as keyboard encoder or other applications.

FEATURES

- Operating voltage range : 4.5V ~ 5.5V.
- Available in temperature range: 0°C ~ 70°C.
- 2K x 13 on chip ROM (EM78248), or
  4K x 13 on chip ROM (EM78448)
- 11 special function registers.
- 146 × 8 general purpose registers (SRAM).
- 5 bi-directional I/O ports (35 I/O pins).
- 3 LED direct sink pins with internal serial resistor.
- Built-in RC oscillator with external serial resistor.
- Built-in power on reset.
- 5 level stack for subroutine nesting.
- 8-bit real time clock/counter (TCC) with overflow interrupt.
- Two oscillator periods option or four oscillator periods per instruction cycle.
- Power down mode.
- Programmable wake up from sleep circuit on I/O ports.
- Programmable free running on-chip watchdog timer.
- 16 pull-up and wake-up pins.
- Two open-drain pins.
- Two R-option pins.
- 40 pin DIP.

PIN ASSIGNMENTS

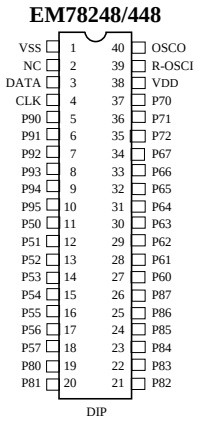


Fig. 1 Pin configuration of EM78248/448

FUNCTIONAL BLOCK DIAGRAM

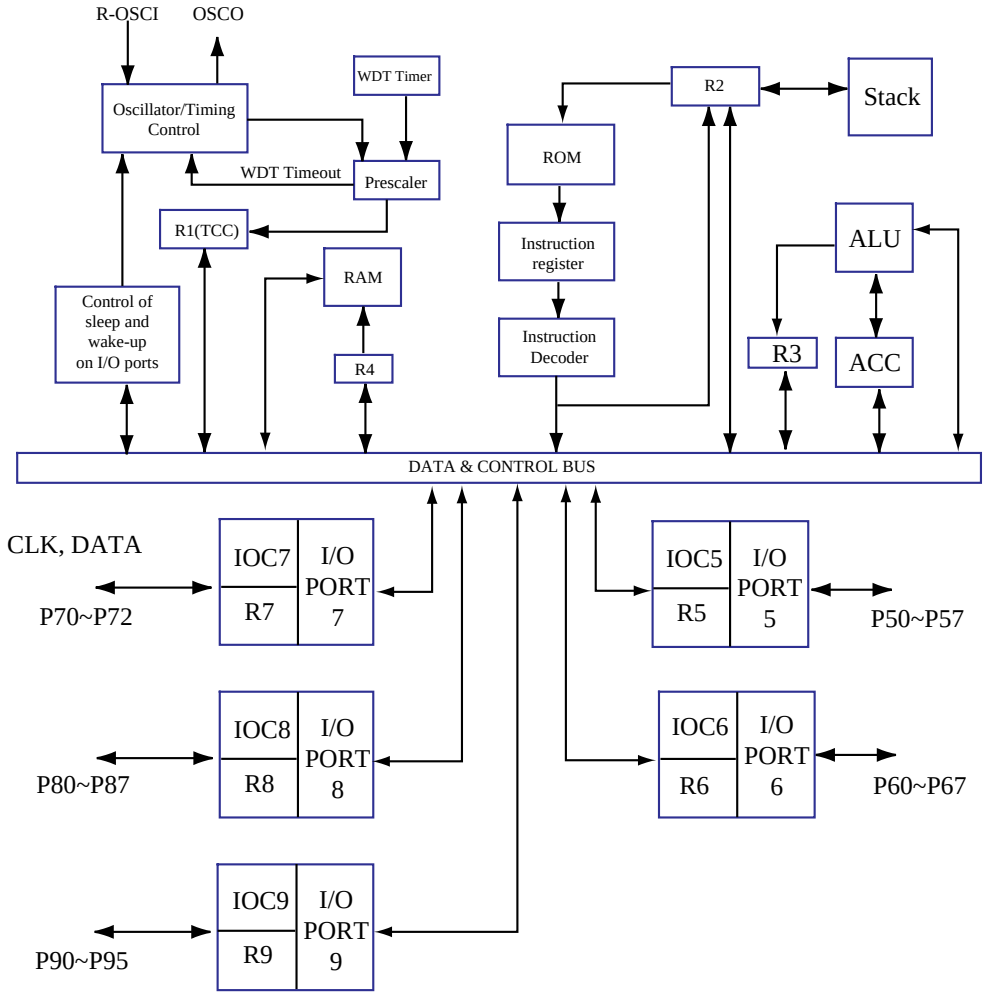


Fig. 2 Functional block diagram

PIN DESCRIPTIONS

Symbol	I/O	Function
R-OSCI	I	56 Kohm±5% pull high for 1.8432MHz.
OSCO	O	Clock output.
P90~P95	I/O	Port 9 is an 6-bit bi-directional I/O port. Can be pulled-high internally by software control.
P80~P87	I/O	Port 8 is an 8-bit bi-directional I/O port. P80 and P81 are also the R-option pins.
P70~P72	I/O	3 LED direct sink pins with internal serial register when use to do output port.
CLK	I/O	P74 and P76 connect together. P74 can be pulled-high internally by software control. P76 can have open-drain output by software control.
DATA	I/O	P75 and P77 connect together . P75 can be pulled-high internally by software control. P77 can have open-drain output by software control.
P60~P67	I/O	Port 6 is an 8-bit bi-directional port. They can be pulled-high internally by software control.
P50~P57	I/O	Port 5 is an 8-bit bi-directional I/O port.
VDD	-	Power supply pin.
VSS	-	Ground pin.

FUNCTION DESCRIPTIONS

Operational Registers

R0 (Indirect Addressing Register)

- R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

R1 (TCC)

- Increased by the instruction cycle clock.
- Written and read by the program as any other register.

R2 (Program Counter) & Stack

- Depending on the device type, R2 and hardware stack are 11/12 bits wide. The structure is depicted in Fig. 3.
- Generates 2K/4K × 13 on-chip ROM addresses to the relative programming instruction codes. One program page is 1K words long.
- R2 is set all “1”s upon a RESET condition.
- ”JMP” instruction allows the direct loading of the lower 10 program counter bits. Thus, “JMP” allows jump to any location on one page.
- “CALL” instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be any location on one page.
- “RET” (“RETL k”, “RETI”) instruction loads the program counter with the contents at the top of stack.
- “MOV R2,A” allows the loading of an address from the “A” register to the lower 8 bits of PC, and the ninth and tenth bits (A8~A9) of PC are cleared.

- "ADD R2,A" allows a relative address be added to the current PC, and the ninth and tenth bits of PC are cleared.
- Any instruction which writes to R2 (e.g. "ADD R2,A", "MOV R2,A", "BC R2,6",·····) (except "TBL") will cause the ninth and tenth bits (A8~A9) of PC to be cleared. Thus, the computed jump is limited to the first 256 locations of any program page.
- "TBL" allows a relative address be added to the current PC (R2+A→R2), and contents of the ninth and tenth bits (A8~A9) of PC are not changed. Thus, the computed jump can be on the second (or third, 4th) 256 locations on one program page.
- In case of EM78248, the most significant bit (A10) will be loaded with the content of bit PS0 in the status register (R3) upon the execution of a "JMP", "CALL", or any instruction which writes to R2.
- In case of EM78448, the most significant bits (A10~A11) will be loaded with the contents of bits PS0~PS1 in the status register (R3) upon the execution of a "JMP", "CALL", or any instruction which writes to R2.

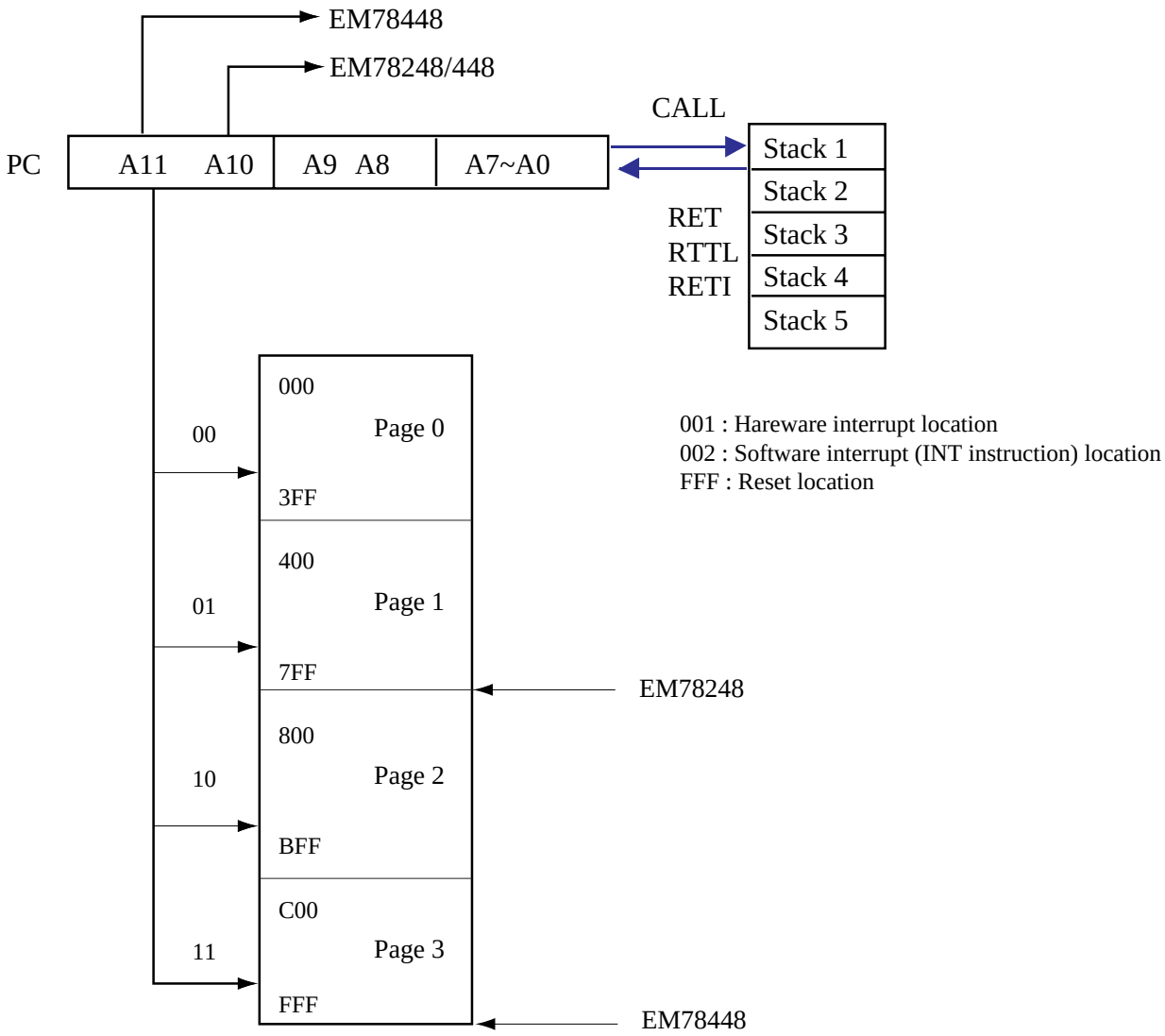


Fig. 3 Program counter organization

R3 (Status Register)

7	6	5	4	3	2	1	0
GP	PS1	PS0	T	P	Z	DC	C

Bit 0 (C) Carry flag

Bit 1 (DC) Auxiliary carry flag

Bit 2 (Z) Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 3 (P) Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4 (T) Time-out bit. Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

Bit 5 (PS0) ~6 (PS1) Page select bits. PS0~PS1 are used to preselect a program memory page. When executing a "JMP", "CALL", or other instruction which causes the program counter to be changed (e.g. MOV R2,A), PS0~PS1 are loaded into the 11th and 12th bits of the program counter, selecting one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS1 bits. That is, the return will be always to the page from where the subroutine was called, regardless of the current setting of PS0~PS1 bits. PS1 bit is not used (read as "0") and cannot be modified in EM78248.

PS1	PS0	Program memory page (Address)
0	0	Page 0 (000-3FF) (EM78248/448)
0	1	Page 1 (400-7FF) (EM78248/448)
1	0	Page 2 (800-BFF) (EM78448)
1	1	Page 3 (C00-FFF) (EM78448)

Bit 7 (GP) General read/write bit.

R4 (RAM Select Register)

- Bits 0~5 are used to select the registers (address: 00~3F) in the indirect addressing mode.
- Bits 6~7 determine which bank is activated among the 4 banks.
- If no indirect addressing is used, the RSR can be used as an 8-bit wide general purpose read/write register.
- See the configuration of the data memory in Fig. 4.

R5~R8 (Port 5 ~ Port8)

- Four 8-bit I/O registers, P74 and P76 read/write data from DATA pin. P75 and P77 read/write data from CLK pin.

R9 (Port 9)

- 6-bit I/O registers. The high order 2 bits of R9 will be read as "0".

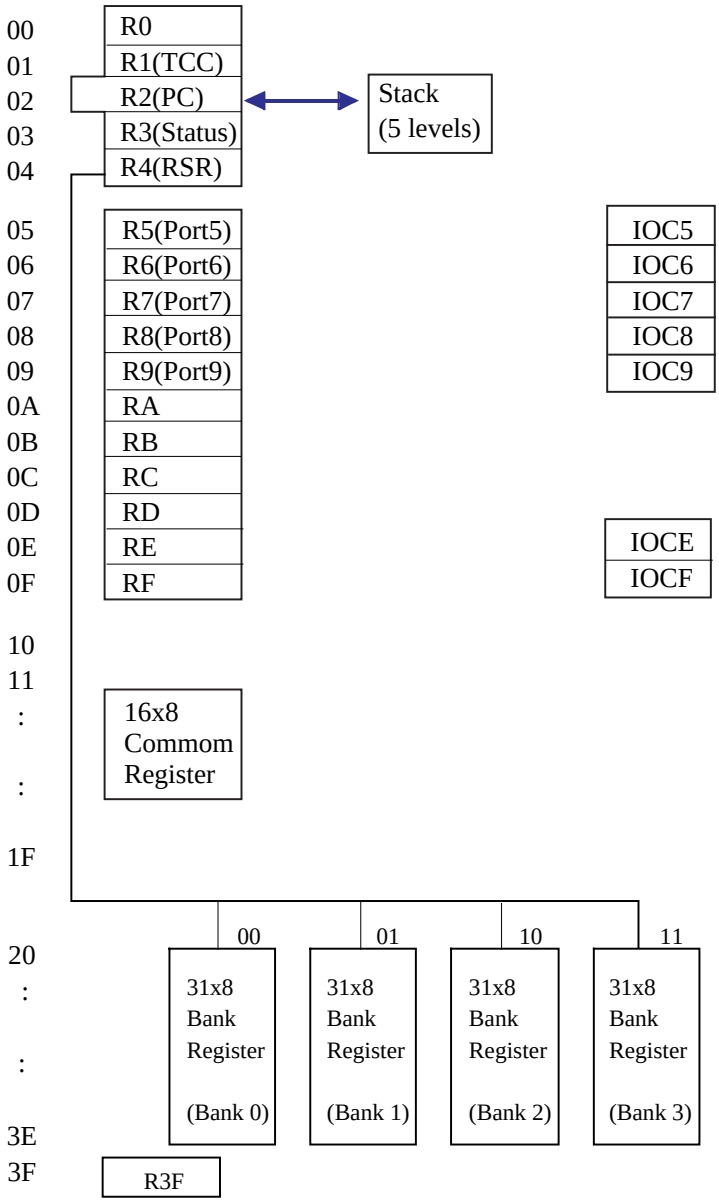


Fig. 4 Data memory configuration

RA ~ R1F, R20~R3E (General Purpose Register)

- RA~R1F and R20~R3E (including Banks 0~3) are general purpose registers.

R3F (Interrupt Status Register)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	TCIF

- **Bit 0 (TCIF)** TCC timer overflow interrupt flag. Set when TCC timer overflows, reset in software.
- **Bits 1~~7** Not used.
- "1" means interrupt request, "0" means non-interrupt.

- R3F can be cleared by instruction and cannot be set by instruction.
- IOCF is the interrupt mask register.
- Note that reading R3F by instruction will get the result of "logic AND" of R3F and IOCF.

Special Purpose Registers

A (Accumulator)

- Internal data transfer, or instruction operand holding.
- It's not an addressable register.

CONT (Control Register)

7	6	5	4	3	2	1	0
$\overline{\text{PHEN}}$	INT	-	-	PAB	PSR2	PSR1	PSR0

Bit 0 (PSR0)~Bit 2 (PSR2) TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3 (PAB) Prescaler assignment bit.
0: TCC
1: WDT

Bit 6 (INT) Interrupt enable flag which cannot be written by CONTW instruction.
0: interrupt masked by DISI.
1 : interrupt enabled by ENI/RETI instruction.

Bit 7 ($\overline{\text{PHEN}}$) I/O pin pull-high enable flag.
0: P60~P67 and P74~P75 and P90~P95 have internal pull-high.
1: pull-high is disabled.

- Bits 0~3, 7 of CONT register are readable and writable.
- Bit 4,5 Not used.

IOC5 ~ IOC9 (I/O Port Control Register)

- "1" put the relative I/O pin into high impedance, while "0" put the relative I/O pin as output.
- IOC5 ~ IOC9 are five I/O direction control registers. Both P74 and P76, P75 and P77 avoid to do output pin at same time. Only lower 6 bits are used in IOC9.

IOCE (WDT Control Register)

7	6	5	4	3	2	1	0
-	ODE	WTE	SLPC	ROC	-	-	$\overline{\text{WUE}}$

Bit 0 ($\overline{WUE}$) Control bit used to enable wake-up function of P60~P67, P74~P75, P90~P91.
0: Enable wake-up function
1: Disable wake-up function
$\overline{WUE}$ bit is readable and writable.

Bit 3 (ROC) ROC is used for the R-option. Setting ROC to "1" will enable the status of R-option pin (P80, P81) to be read by the controller. Clearing ROC will disable the R-option function. If the R-option function is used, the user must connect the P81 pin or/and P80 pin to VSS by a 560KΩ external resistor (Rex). If Rex is connected/disconnected, the status of P80(P81) will be read as "0"/"1" when ROC is set to "1". Refer to Fig. 7(b). ROC bit is readable and writable.

Bit 4 (SLPC) This bit is set by hardware at the falling edge of wake-up signal and is cleared by software. SLPC is used to control the operation of oscillator. The oscillator is disabled (oscillator is stopped, the controller enters the SLEEP2 MODE) on high-to-low transition on SLPC bit and is enabled (the controller is awakened from SLEEP2 MODE) on low-to-high transition on SLPC bit. In order to ensure the stable output of the oscillator, once the oscillator is disabled and is enabled again, there is a delay for approximately 18 ms (oscillator start-up timer, OST) before the next instruction of program being executed. The OST is always activated by wake-up from sleep mode whether the Code Option bit WTC is "0" or not. After waking up, the WDT is enabled if Code Option WTC is "1". The block diagram of SLEEP2 MODE and wake-up caused by input triggered is depicted in Fig. 5. SLPC bit is readable and writeable.

Bit 5 (WTE) Control bit used to enable Watchdog timer.
WTE bit is used only if the CODE Option bit WTC is "1". If WTC bit is "1", then WDT is disabled/enabled by WTE bit.
0: Disable WDT
1: Enable WDT
WTE bit is not used if the CODE Option bit WTC is "0". That is, if WTC bit is "0", WDT is always disabled no matter what the WTE bit is.
WTE bit is readable and writable.

Bit 6 (ODE) Open-drain control bit.
0: Both P76 and P77 are normal I/O pins.
1: Both P76 and P77 pins have open-drain output, but built-in internally.
ODE bit is readable and writable.

Bits 1,2,7 Not used.

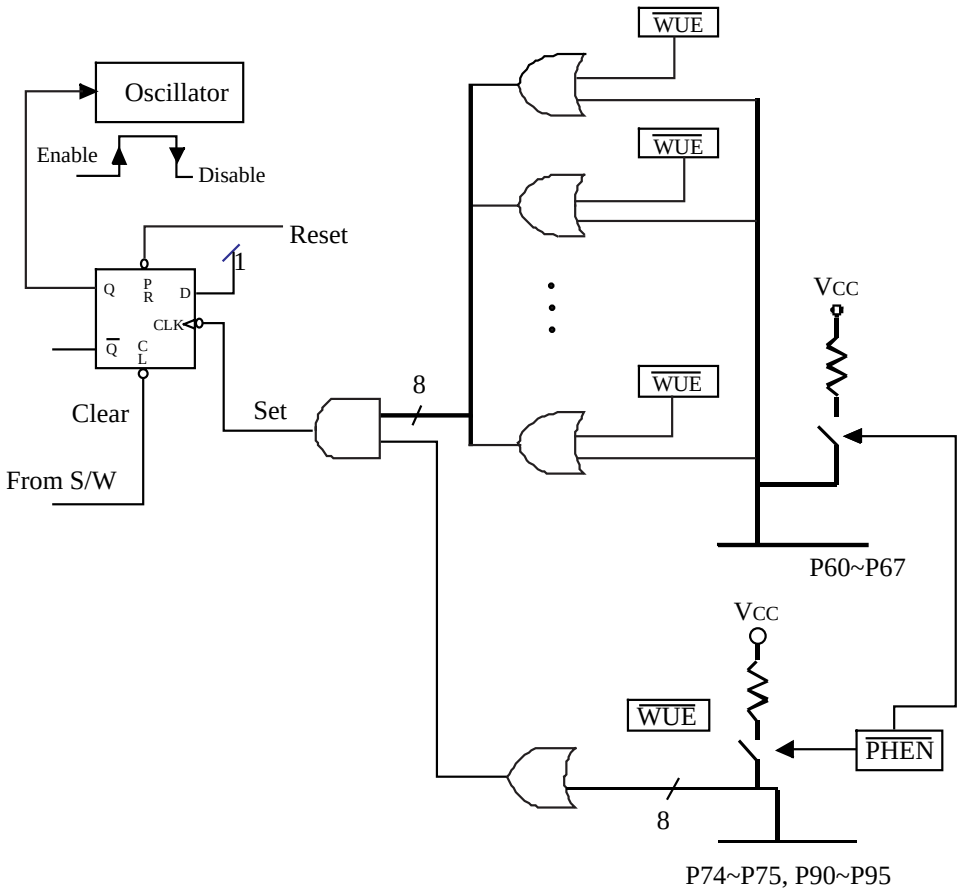


Fig. 5 Block diagram of sleep mode and wake-up circuits on I/O ports

IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	TCIE

Bit 0(TCIE) TCIF interrupt enable bit.
0: disable TCIF interrupt.
1: enable TCIF interrupt.
Bits 1~7 Not used.

- Individual interrupt is enabled by setting its associated control bit in IOCF to "1".
- IOCF Register is readable and writable.

TCC/WDT Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time and the PAB bit of CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the prescale ratio. The prescaler will be cleared by instructions which write to TCC each time, when assigned to TCC mode. The WDT and prescaler, when assigned to WDT mode, will be cleared by the WDTC and SLEP instructions. Fig. 6 depicts the circuit diagram of TCC/WDT.

- R1(TCC) is an 8-bit timer/counter. TCC will increase by one in every instruction cycle (without prescaler).
- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep running even the oscillator driver has been turned off (i.e. in sleep mode). During the normal operation or the sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming (if Code Option bit WTC is "1"). Refer to WTE bit of IOCE register. With no presacler, the WDT time-out period is approximately 18 ms.

I/O Ports

The I/O registers, Port 5 ~ Port 9, are bi-directional tri-state I/O ports. P60~P67, P74~P75, P90~P91 can have internal pull-high and wake-up function by software control. P76~P77 can have open-drain output by software control. P80~P81 are the R-option pins which are enabled by software. While R-option function is used, P80~P81 are recommended to be used as output pins. During the period of R-option being enabled, P80~P81 must be programmed as input pins. If external resistor is connected to P80(P81) for R-option function, the current consumption should be noticed in the applications that low power are concerned.
The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC5~IOC9) under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig. 7. Note that the source is different between the reading path of input and output pin while reading the I/O port.

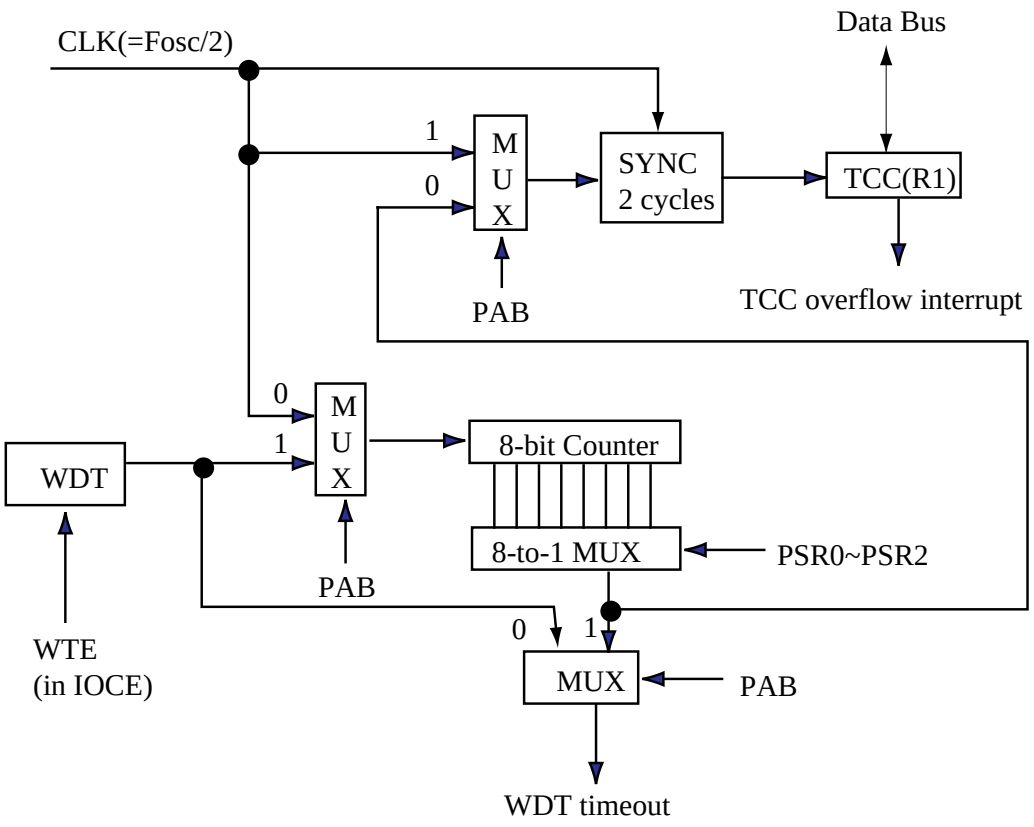


Fig. 6 Block diagram of TCC and WDT

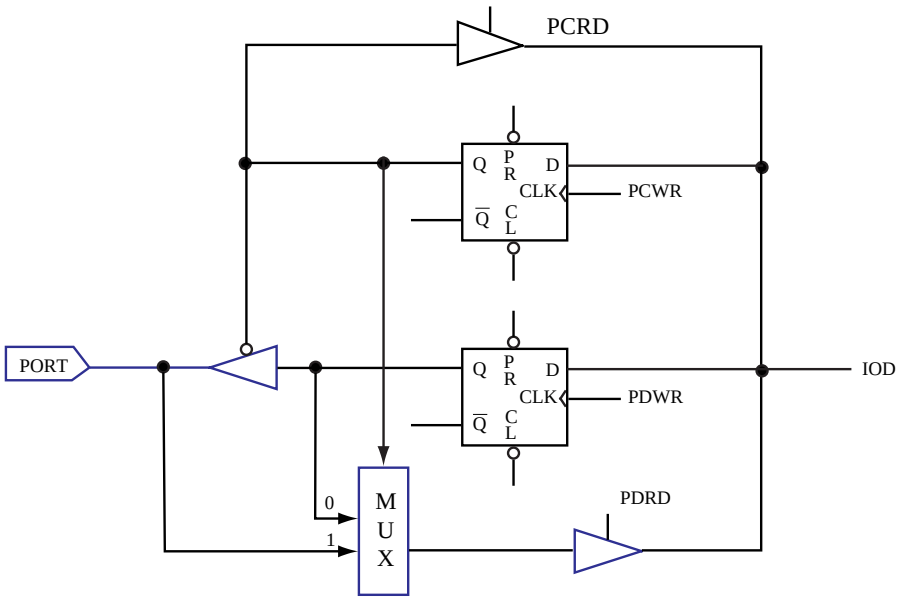
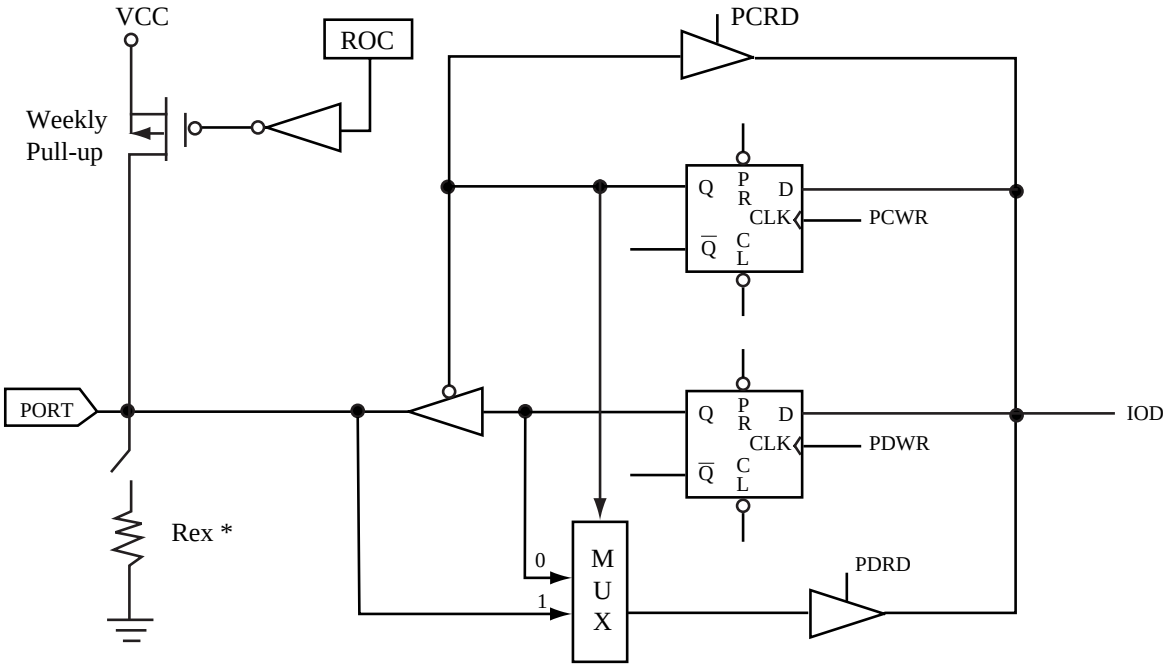


Fig. 7(a) The circuit of I/O port and I/O control register



* The Rex is 560K ohm external resistor.

Fig. 7(b) The circuit of I/O port with R-option (P80,P81)

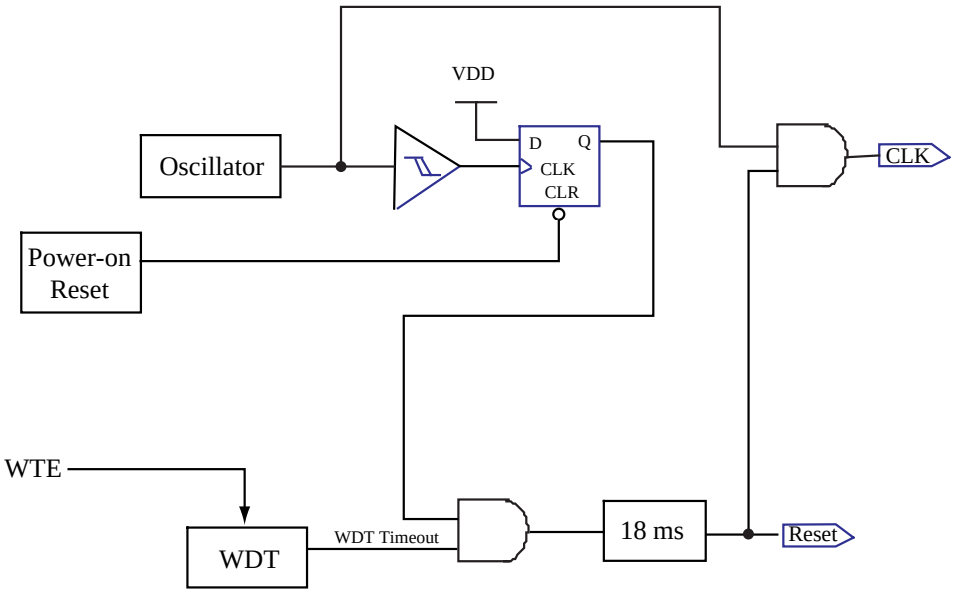


Fig. 8 The Block diagram of Reset of controller

RESET and Wake-up

The RESET can be caused by
(1) Power on reset, or
(2) WDT timeout. (if enabled)

The device will be kept in a RESET condition for a period of approx. 18ms (one oscillator start-up timer period) after the reset is detected. Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "1''.
- When power on, Bits 5~6 of R3 and the upper 2 bits of R4 are cleared.
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is enabled if Code Option bit WTC is "1''.
- The CONT register is set to all "1" except bit 6 (INT flag).
- Bits 3,6 of IOCE register are cleared, bits 0,4~5 of IOCE register are set to "1''.
- Bits 0 of R3F and bits 0 of IOCF registers are cleared.

The sleep mode (power down mode) can be entered by executing the SLEP instruction (named as SLEEP1 MODE). While entering sleep mode, the WDT (if enabled) is cleared but keeping running. The controller can be awakened by WDT timeout (if enabled), and it will cause the controller to be reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up).

In addition to the basic SLEEP1 MODE, EM78248/448 has another sleep mode (caused by clearing "SLPC" bit of IOCE register, named as SLEEP2 MODE). In the SLEEP2 MODE, the controller can be awakened by

(a) input triggered, refer to Fig. 5. When wake-up, the controller will continue to execute program in-line. In this case, before entering SLEEP2 MODE, the wake-up function of the trigger sources (P60~P67, P74~P75, and P90~P91) should be selected (e.g. input pin) and enabled (e.g. pull-high, wake-up control). One

caution should be noted is that after waking up, the WDT is enabled if Code Option bit WTC is "1". The WDT operation (to be enabled or disabled) should be appropriately controlled by software after waking up.

(b) WDT time-out (if enabled). When wake-up, will cause the controller reset.

Interrupt

The EM78248/448 has the TCC overflow interrupts.

R3F is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 001H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the R3F register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

The flag in the Interrupt Status Register (R3F) is set regardless of the status of its mask bit or the execution of ENI instruction. Note that reading R3F will get the output of logic AND of R3F and IOCF. Refer to Fig. 9. The RETI instruction exits interrupt routine and enables the global interrupt (execution of ENI instruction). When an interrupt is generated by INT instruction (when enabled), causes the next instruction to be fetched from address 002H.

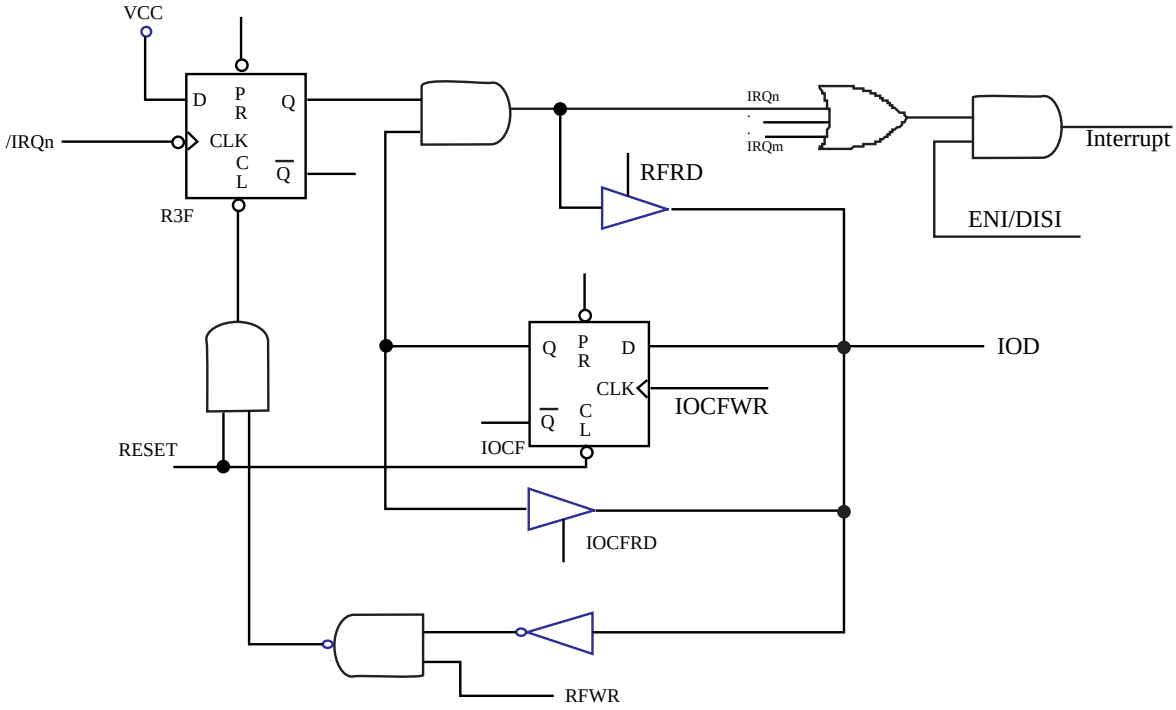


Fig. 9 Interrupt input circuit

Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. All instructions are executed within one single instruction cycle (consists of 2 oscillator periods), unless the program counter is changed by

(a) executing the instruction "MOV R2,A", "ADD R2,A", "TBL", or any instruction which writes to R2 (e.g. "SUB R2,A", "BS R2,6", "CLR R2", ····).

(b) CALL, RET, RETI, RETL, JMP, Conditional skip (JBS, JBC, JZ, JZA, DJZ, DJZA) tested to be true.

In these cases, the execution takes two instruction cycles.

In addition, the instruction set has the following features:

(1). Every bit of any register can be set, cleared, or tested directly.

(2). The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register.

The symbol "R" represents a register designator which specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	HNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <Note1>
0 0000 0010 0000	0020	TBL	R2+A → R2, Bits 8~9 of R2 unchanged	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC

INSTRUCTION BINARY	HEX	HNEMONIC	OPERATION	STATUS AFFECTED
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None <Note2>
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None <Note3>
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0010	1E02	INT	PC+1 → [SP], 002H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

<Note1> This instruction can operate on IOC5~IOC9, IOCE~IOCF only.
<Note2> This instruction is not recommended to operate on R3F.
<Note3> This instruction cannot operate on R3F.

CODE Option Register

The EM78248/448 has one CODE option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

7	6	5	4	3	2	1	0
-	-	-	CK2	-	WTC	-	-

Bit 2 (WTC): WDT option.
0: WDT is always disabled. Control bit WTE in IOCE is unused.
1: WDT is enabled. WDT can be disabled/enabled by software programming. Control bit WTE in IOCE register is used to disable/enable WDT.

Bit 4 (CK2): Input clock divided by two selection.
0: System clock is from oscillator clock directly.
1: System clock is from oscillator clock divided by two.

Bits 0~1, 3, 5~7: Not used, must be “0”s.

ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Condition	Rating
Temperature under bias	T_{OPR}		0°C to 70°C
Storage temperature	T_{STR}		-65°C to 150°C
Input voltage	V_{IN}		-0.3V to +6.0V
Output voltage	V_O		-0.3V to +6.0V

DC ELECTRICAL CHARACTERISTIC (T_A=0°C ~ 70°C, V_{DD}=5.0V, V_{SS}=0V)

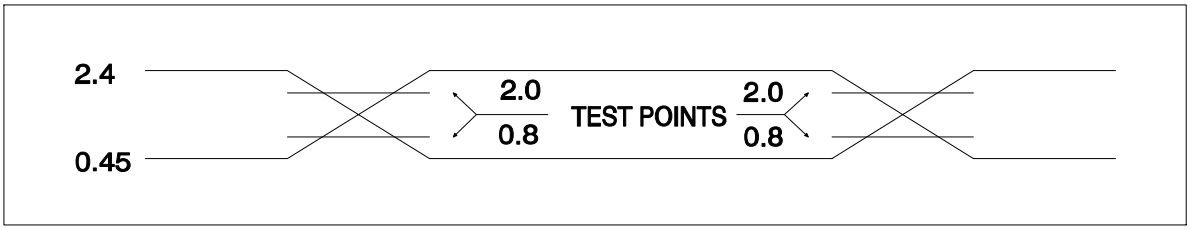
Parameter	Sym.	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{IL1}	$V_{IN} = V_{DD}, V_{SS}$			±1	μA
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Clock Input High Voltage	V_{IHX}	OSCI	3.5			V
Clock Input Low Voltage	V_{ILX}	OSCI			1.5	V
Output High Voltage (Port 5,6,8,9 and P74~P77)	V_{OH1}	I_{OH} = -12.0mA	2.4			V
Output High Voltage (P70~P72)	V_{OH2}	I_{OH} = -10.0mA	2.4			V
Output Low Voltage (Port 5,6,8,9 and P74~P77)	V_{OL1}	I_{OL} = 5.0mA			0.4	V
Output Low Voltage (P70~P72)	V_{OL2}	I_{OL} = 10.0mA			0.4	V
Pull-high current	I_{PH}	Pull-high active, input pin at V_{SS}	-250	-400	-500	μA
Power down current	I_{SB}	All input and I/O pins at V_{DD}, output pin floating, WDT enabled			10	μA
Operating supply current	I_{CC1}	$\overline{RESET}$='High', Fosc=1.84324MHz (CK2="0"), output pin floating			3	mA

AC ELECTRICAL CHARACTERISTICS (T_A=0°C ~ 70°C, V_{DD}=5.0V, V_{SS}=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time (CK2="0")	Tins	RC Type	500		DC	ns
TCC input period	Ttcc		(Tins+20)/N*			ns
Watchdog timer period	Twdt	Ta = 25°C		18		ms
Device reset hold period	Tdrh	Ta = 25°C		18		ms

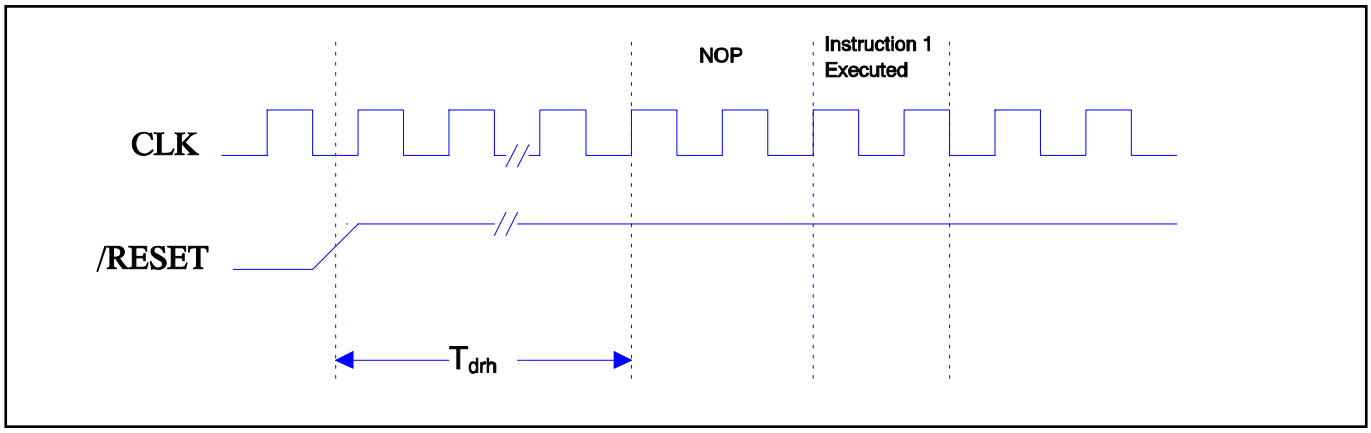
* N= selected prescaler ratio.

AC Test Input/Output Waveform

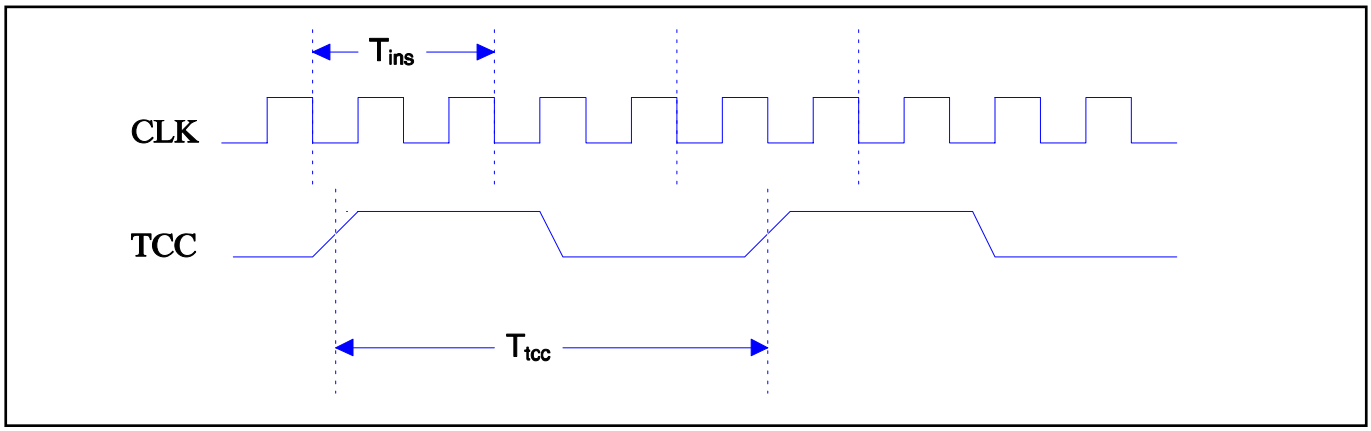


AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing (CK2="0")



TCC Input Timing (CK2="0")



APPLICATION CIRCUIT